# Cyclone III FPGA Starter Kit

# User Guide

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# Contents

## Chapter 5. Appendix: Programming the Configuration Flash Device

# About this User Guide

This user guide describes how to start using the Altera® Cyclone® III FPGA Starter Kit, including unpacking the kit, installing required software, connecting the development board to a PC, and running sample software.

For a full description of the development board and its use, refer to the *Cyclone III FPGA Starter Board Reference Manual*.

To ensure that you have the most up-to-date information on this product, go to the Altera website at **www.altera.com/products/devkits/altera/kit-cyc3-starter.html**.

## Revision History

The table below displays the revision history for the chapters in this user guide.

| Chapter | Date | Version | Changes Made |
|---|---|---|---|
| 1 | April 2007 | 1.0.0 | • First publication. |

## How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

| Information Type | Contact *Note (1)* |
|---|---|
| Technical support | www.altera.com/mysupport/ |
| Technical training | www.altera.com/training/ |
| Technical training services | custrain@altera.com |
| Product literature | www.altera.com/literature |
| Product literature services | literature@altera.com |
| FTP site | ftp.altera.com |

***Note to table:***
(1) You can also contact your local Altera sales office or sales representative.

# Typographic Conventions

This document uses the typographic conventions shown below.

| Visual Cue | Meaning |
|---|---|
| **Bold Type with Initial Capital Letters** | Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box. |
| **bold type** | External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file. |
| *Italic Type with Initial Capital Letters* | Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.* |
| *Italic type* | Internal timing parameters and variables are shown in italic type. Examples: $t_{PIA}$, $n + 1$.<br><br>Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file. |
| Initial Capital Letters | Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu. |
| "Subheading Title" | References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions." |
| `Courier type` | Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`.<br><br>Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier. |
| 1., 2., 3., and<br>a., b., c., etc. | Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure. |
| ■ ● • | Bullets are used in a list of items when the sequence of the items is not important. |
| ✓ | The checkmark indicates a procedure that consists of one step only. |
|  | The hand points to information that requires special attention. |
|  | A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work. |
|  | A warning calls attention to a condition or possible situation that can cause injury to the user. |
| ↵ | The angled arrow indicates you should press the Enter key. |
|  | The feet direct you to more information on a particular topic. |

# 1. Getting Started

## Introduction

Welcome to the Altera® Cyclone® III FPGA Starter Kit, which includes a full-featured field-programmable gate array (FPGA) development board, hardware and software development tools, documentation, and accessories needed to begin FPGA development.

The development board includes an Altera Cyclone III FPGA and comes preconfigured with a hardware reference design stored in flash memory. Hardware designers can use the development board as a platform to prototype a variety of FPGA designs.

The kit provides an integrated control environment that includes a software controller in control panel application, a USB command controller, a multi-port SRAM/DDR SDRAM/flash memory controller, and demonstration circuitry specified in Verilog code. This design is provided as a starting point for test designs so users can get up and running quickly. This user guide addresses the following topics:

- How to set up, power up, and verify correct operation of the development board
- Where to get and how to install the Altera Development Suite Tools
- How to install the *Cyclone III FPGA Starter Kit* CD-ROM
- How to set up and use the control panel, a graphical user interface (GUI), to manipulate components on the board, implement applications, and display images on a VGA monitor.
- How to configure the Cyclone III FPGA
- How to set up and run application examples.

For complete details on the development board, refer to the *Cyclone III FPGA Starter Board Reference Manual*.

## Before You Begin

Before proceeding, check the contents of the kit:

- Cyclone III FPGA Starter Development Board
- *Cyclone III FPGA Starter Kit* CD-ROM containing the development board documentation and supporting materials, including the user guide and reference manual, control panel utility, design examples, device datasheets, and tutorials.
- 12 V DC power supply
- USB cable

## Further Information

For other related information, refer to the following websites:

- For additional daughter cards available for purchase:

  www.altera.com/products/devkits/kit-daughter_boards.jsp

- For the Cyclone III handbook:

  www.altera.com/literature/lit-cyc3.jsp

- For the Cyclone III reference designs:

  www.altera.com/endmarkets/refdesigns/device/cyclone3/cyclone3-index.jsp

- For eStore if you want to purchase devices:

  www.altera.com/buy/devices/buy-devices.html

- For Cyclone III Orcad symbols:

  www.altera.com/support/software/download/pcb/pcbpcb_index.html

- For Nios® II 32-bit embedded processor solutions:

  www.altera.com/technology/embedded/emb-index.html

## Software Installation

The instructions in this section describe how to install the following software:

- *Cyclone III FPGA Starter Kit* CD-ROM
- The Quartus® II Software, Development Kit Web Edition

### Installing the Cyclone III FPGA Starter Kit CD-ROM

The *Cyclone III FPGA Starter Kit* CD-ROM contains the following items:

- The kit's design examples and board design files
- *Quick Start Guide*
- *My First FPGA Tutorial*
- *Cyclone III FPGA Starter Kit User Guide* (this document)
- *Cyclone III FPGA Starter Board Reference Manual*

To install the *Cyclone III FPGA Starter Kit* CD-ROM, perform the following steps:

1. Insert the *Cyclone III FPGA Starter Kit* CD-ROM into the CD-ROM drive.

   The CD-ROM should start an auto-install process. If it does not, browse to the CD-ROM drive and double-click on the **setup.exe** file.

2. Follow the online instructions to complete the installation process. The installation program creates shortcuts in the Windows Start Menu at: **All Programs > Altera > Cyclone III FPGA Starter Kit v7.1.0**. Use this icon to launch the Windows-style development kit GUI or view the documentation.

The Cyclone III FPGA Starter Kit installation program creates a directory structure for the installed files (Figure 1–1), where <*path*> is the selected Cyclone III Starter Kit installation directory.

***Figure 1–1. Cyclone III Starter Kit Installed Directory Structure***

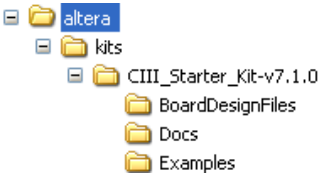



Table 1–1 lists the file directory names and a description of their contents.

***Table 1–1. Installed Directory Contents***

| Directory Name | Description of Contents |
|---|---|
| BoardDesignFiles | Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design. |
| Docs | Contains the development kit documentation. |
| Examples | Contains the design exmaple files for the Cyclone III FPGA Starter Kit |

## Installing the Quartus II Software

Download and install the *Quartus II Web Edition* software by performing the following steps:

1. From the Altera website home page (**www.altera.com**), click **Download**.
2. Follow the online instructions to complete the installation process.

☞ If you have difficulty installing the Quartus II software, refer to *Installing the Quartus II Software* in the *Quartus II Installation & Licensing Manual for PCs* found at **www.altera.com**.

The Quartus II software is the primary FPGA development tool used to create the reference designs used in this development kit.

Additionally, you may want to install the *Nios II Embedded Design Suite* package also found in the *Altera Design Software Suite*. The Nios II soft-core embedded processor runs on Altera FPGAs. Some of the reference designs included in this development kit use the Nios II processor.

## Licensing the Quartus II Software

Before using the Quartus II software, you must request a license file from the Altera website at www.altera.com/licensing and install it on your PC. When you request a license file, Altera e-mails you a license.dat file that enables the software. To obtain a license, perform the following steps:

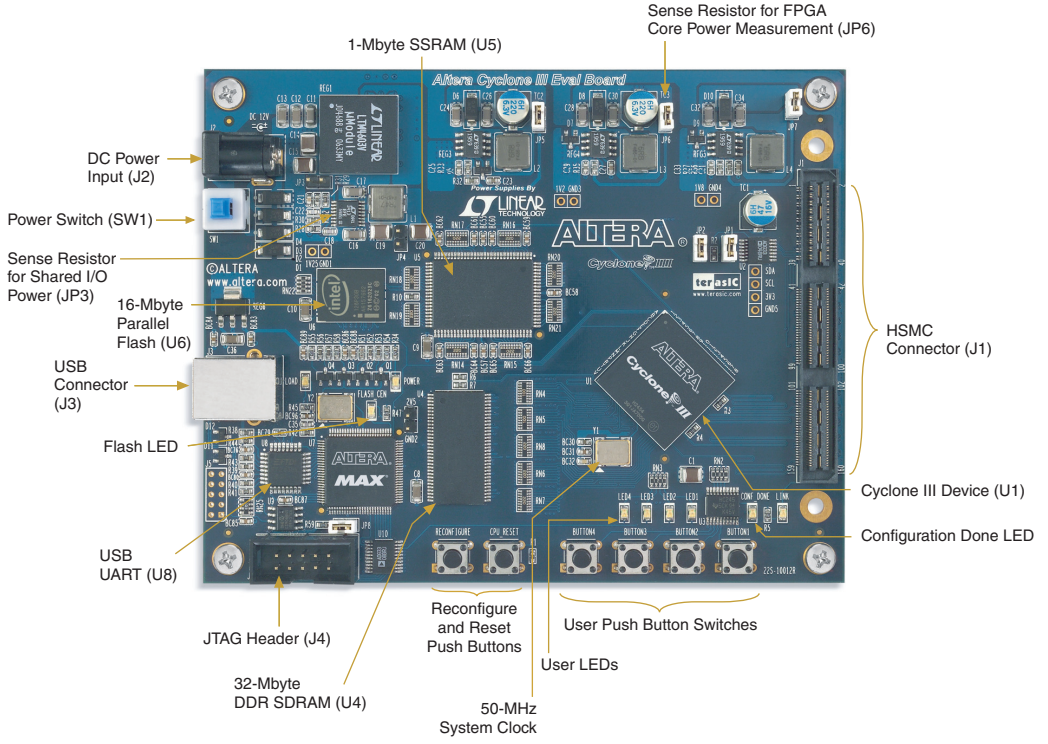
1. Go to the Altera website at www.altera.com/licensing.
2. Click Quartus II Web Edition Software.
3. Follow the on-line instructions to request your license. A license file is e-mailed to you. Save this file on your computer.
4. Run the Quartus II software.
5. Choose **License Setup** (Tools menu).
6. Under **License File**, indicate the license file you received and saved onto your computer in step 3.

# 2. Development Board & Control Panel Setup

## Development Board Setup

The development board is preloaded with a configuration to demonstrate Cyclone® III device and board features. At power up, the preloaded configuration also enables users to quickly confirm that the board is operating correctly. See Figure 2–1.

*Figure 2–1. Cyclone III Development Board Layout and Components*



### Requirements

If not already installed, you should:

- Install the Altera® Quartus® II software on the host computer
- Install the *Cyclone III FPGA Starter Kit* CD ROM
- Install the USB-Blaster™ driver software on the host computer. The Cyclone III FPGA starter development board includes integrated USB-Blaster circuitry for FPGA programming.

Communication between the host computer and the development board requires that the USB-Blaster driver software be pre-installed.

### Powering Up the Development Board

To power up the development board, perform the following steps:

1. Ensure that the on/off switch (SW1) is in the *OFF* position (up).
2. Connect the USB-Blaster cable from the host computer to the USB-Blaster port on the development board.
3. Connect the 12 V DC adapter to the development board and to a power source.

WARNING

Only use the supplied 12 V power supply. Power regulation circuitry on the board could be damaged by supplies greater than 12 V.

4. Press the **Power Switch** (SW1).
5. Confirm that all user LEDs are flashing in a "counting" pattern.

## Control Panel Setup

The kit's control panel enables access to board components via a host computer through the USB connection.

For more information about using the control panel, refer to the "Using the Control Panel" chapter.

Setting up the control panel involves the following:

- Configuring the FPGA
- Starting the control panel

At this point, the Quartus II software and the USB-Blaster driver software should be installed. In addition, the development board should be powered up and working.

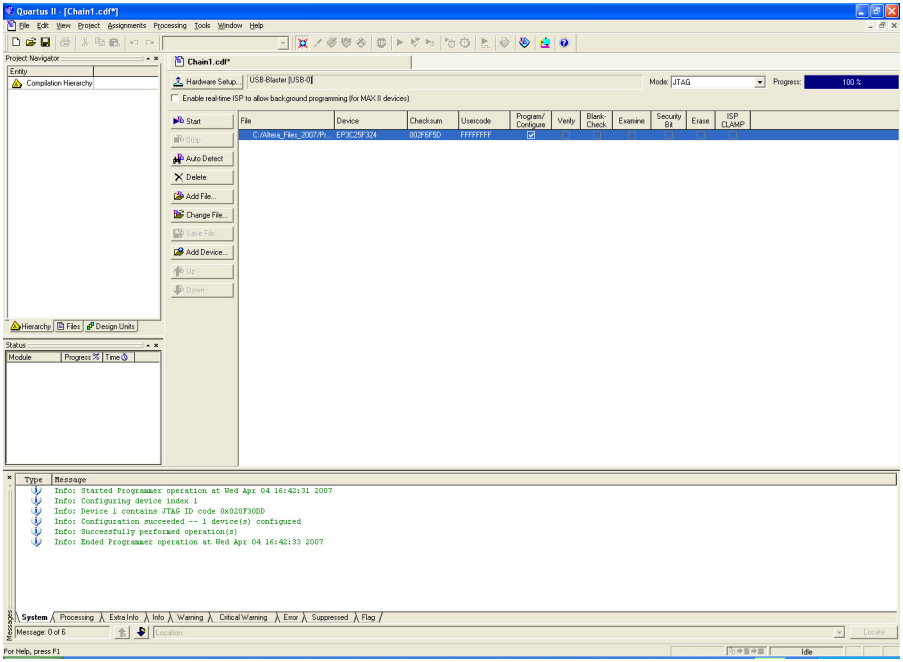
## FPGA Configuration

Before using the control panel, configure a corresponding circuit in the Cyclone III FPGA by downloading the **CIII_Control_Panel.sof** configuration file from the *<kit path>***Examples****CIII_Control_Panel****HW** directory.

To configure the Cyclone III device, perform the following steps:

1. Start the Quartus II software.
2. On the Tools menu, click **Programmer**. See Figure 2–2.

***Figure 2–2. Quartus II Programmer Window***



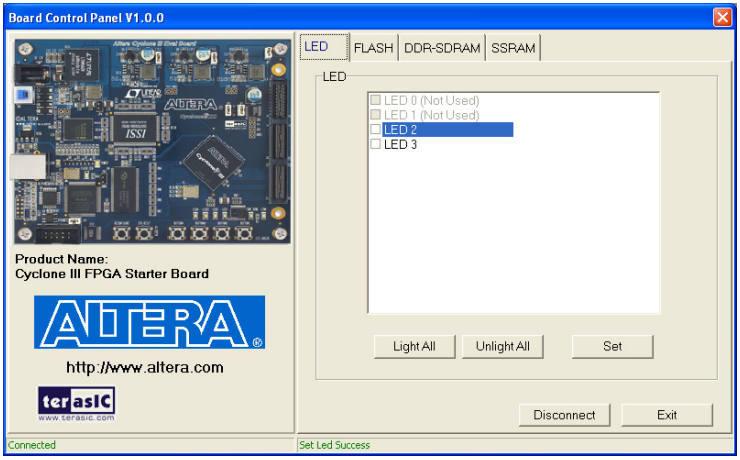
3. Click **Add File** and select **CIII_Control_Panel.sof.**
4. Turn on the **Program/Configure** box to select the added file.
5. Click **Start** to download the selected configuration file to FPGA.

## Control Panel Start

To start the control panel, perform the following step:

✓ To launch the control panel user interface, run the **CIII_Starter_control_panel.exe** program found in the <*kit path*>**\Examples\CIII_Control_Panel\SW** directory (Figure 2–3).

***Figure 2–3. Control Panel Window***



# 3. Using the Control Panel

## Overview

The control panel consists of:

- The graphical user interface (GUI) on the host computer
- Circuitry (specified in Verilog HDL code) downloaded to the board's Cyclone® III device

After the kit's CD-ROM is installed, the control panel hardware and software can be found in the *<kit path>***Examples****CIII_Control_Panel** directory. The Verilog HDL code enables experienced users to change the control panel's functionality.

The design downloaded to the Cyclone III device implements a command controller that processes board commands sent over the USB Blaster from the control panel. To perform the appropriate actions, the command controller communicates with the controller of the targeted board input/output (I/O) device.

You can perform the following actions with the control panel:

- Light up LEDs
- Read from and write to the DDR SDRAM, SRAM, and flash memory

The following sections describe how to perform these actions with the control panel already open on the host computer. If not already open, launch the control panel as described in "Control Panel Start" on page 2–4.

## LEDs

Typical design activities do not require the ability to set arbitrary values for simple display devices. However, for troubleshooting purposes, setting arbitrary values enables you to verify that the devices are operating correctly.

### Illuminating LEDs

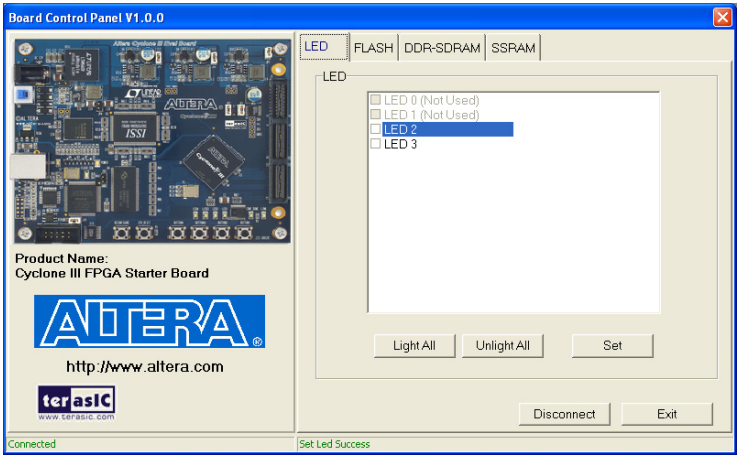
To illuminate an LED, perform the following steps:

1. Click the **LED** tab (Figure 3–1).
2. In the **LED** window, turn on the individual LEDs.

3. Click **Set**.

The Cyclone III starter board uses all of the I/Os in the 324 pin package. Although there are 4 LEDs on the board, when the DDR core is instantiated, the Quartus II software requires 2 of these I/Os to remain unused. This is why you can only control 2 of the LEDs through the control panel.

*Figure 3–1. Control Panel Window for LED Controls*




## DDR SDRAM/ SSRAM Controller and Programmer

You can perform the following types of memory read/write operations with the control panel:

- Read from and write to the DDR SDRAM or SSRAM device
- Write sequential data, or the entire contents of a file, to the DDR SDRAM or SSRAM device
- Read sequential data, or the entire contents of the DDR SDRAM or SSRAM device, to a file

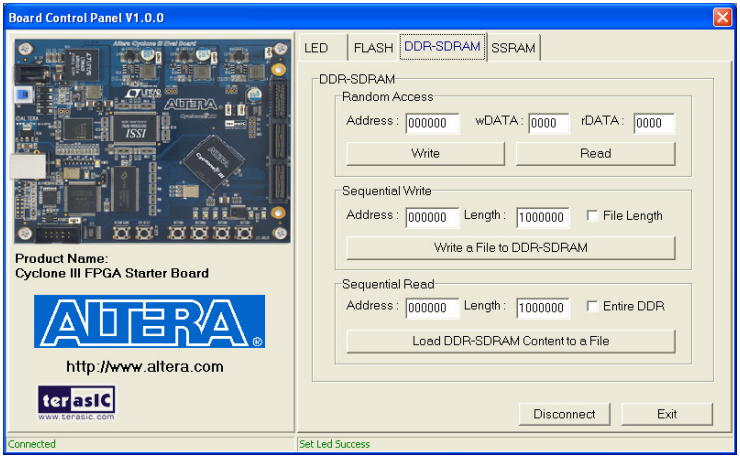
The following sections describe how to access the DDR SDRAM; the same approach also applies to accessing the SSRAM.

## Read/Write Data

To read from and write to the DDR SDRAM, perform the following steps:

1. Click the DDR **SDRAM** tab (Figure 3–2).

*Figure 3–2. Control Panel SDRAM Tab*




2. To write a 16-bit word to the DDR SDRAM, type the hex address of the desired location in the **Random Access** boxes and write the hex data to be written. Click **Write**.

3. To read the contents of a location, enter the address in the **Random Access** boxes. Click **Read**.

## Sequential Write

To write the contents of a file to the DDR SDRAM, perform the following steps:

1. Click the **SDRAM** tab and indicate your preferences using the **Sequential Write** boxes.

2. Type the starting address in the **Address** box.

3. Type the number of bytes to write in the **Length** box.

To load the entire file, turn on **File Length** without specifying the number of bytes.

4. Click **Write a File to DDR SDRAM** to initiate the transaction.

5. Specify the source file in the pop-up Windows dialog box.

### Sequential Read

To read the contents of the DDR SDRAM and write them to a file, perform the following steps:

1. Click the **DDR SDRAM** tab indicate your preferences using the **Sequential Read** boxes.

2. Type the starting address in the **Address** box.

3. Type the number of bytes to copy into the file in the **Length** box.

   To copy the entire contents of the SDRAM into a file, turn on **Entire DDR SDRAM** without specifying the number of bytes.

4. Click **Load DDR SDRAM Content to a File** to initiate the transaction.

5. Specify the destination file in the pop-up Windows dialog box.

## Flash Memory Programmer

Using the control panel, you can perform the following operations to read from and write to the board's flash memory:

- Erase the entire flash memory
- Write one byte to flash memory
- Read one byte from flash memory
- Write a binary file to flash memory
- Load the contents of the flash memory into a file

When performing these transactions, consider the following characteristics and limitations of the flash memory:

- Erasure of the entire flash memory is required before you can write new data
- Flash memory tolerates only a limited number of erasures

CAUTION

Do not exit from the control panel while erasing the entire contents of the flash memory; this takes about 2 minutes.

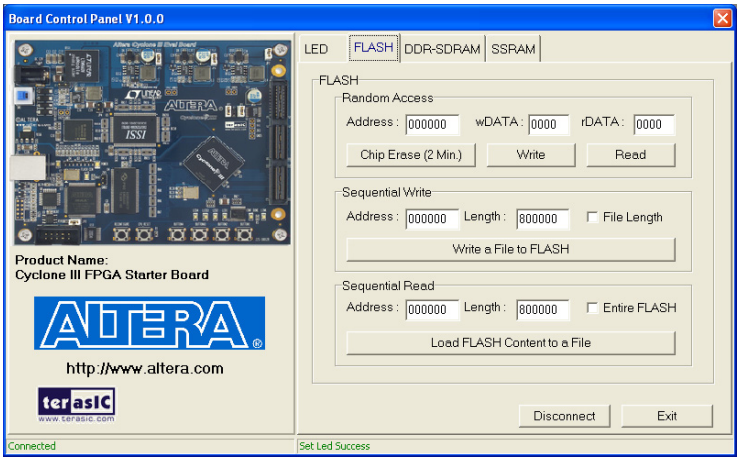
The feature of reading from or writing a byte to an entire file to the flash memory enables you to develop multimedia applications (for example, Flash Audio Player, Flash Picture Viewer) without having to build a flash memory programmer.

## Read/Write Data

To perform a read/write operation with a byte of data from/to the flash memory, perform the following steps:

1. Click the **FLASH** tab (Figure 3–3) and type the data in the **Random Access** boxes.

*Figure 3–3. Control Panel Flash Tab*




2. Click **Chip Erase (2 Min)**. Wait for the operation to finish by observing the button and window frame title prompt. This takes about 2 minutes.

3. Type the desired address in the **Address** box and the data byte in the **wDATA** box.

4. Click **Write**.

5. To read a byte of data from a random location, enter the desired address and click **Read**. The **rDATA** box displays the content of the specified address.

## Sequential Write

To write the contents of a file into flash memory, perform the following steps:

1. Click the **FLASH** tab and type the data in the **Sequential Write** boxes.
2. Under **Random Access**, click **Chip Erase (2 Min)**. Wait for the operation to finish by observing the button and window frame title prompt. This takes about 2 minutes.
3. Under **Sequential Write**, type the starting address in the **Address** box.
4. Specify the number of bytes to write in the **Length** box.

   To load the entire file, turn on **File Length** without specifying the number of bytes.

5. Click **Write a File to FLASH** to initiate the transaction.
6. Specify the source file in the Windows pop-up dialog box.

## Sequential Read

To read the contents of the flash memory and write them to a file, perform the following steps:

1. Click the **FLASH** tab and type the data in the **Sequential Read** boxes.
2. Type the starting address in the **Address** box.
3. Type the number of bytes to read from flash memory in the **Length** box.

   To copy the entire contents of flash memory into a file, turn on **Entire Flash** without specifying the number of bytes.

4. Click **Load FLASH Content to a File**.
5. Specify the destination file in the Windows pop-up dialog box.

# 4. Measuring Power on the Cyclone III Starter Board

## Introduction

One of the main features of the Cyclone® III device is its low power consumption. You can measure the power of the 3C25 device on the Cyclone III starter board under various conditions with a design example provided with the kit.

The power example is designed to allow you to control the amount of logic utilized in the FPGA, the clock frequency, and a number of I/Os being used and measure the effect on the power to the Cyclone III device. Because the Cyclone III starter board has only four buttons and four LEDs, interaction with the board is minimal as defined below.

Table 4–1 describes the functionality of the four input buttons that control the power example.

*Table 4–1. Four Input Button Functionality*

| Button | FPGA Pin | Type | Description |
|---|---|---|---|
| 1 | F1 | Reset | Resets the demo to the beginning, node `i_nrst`. |
| 2 | F2 | Toggle | Advances the design example to the next higher frequency, node `i_nfreq_next`. |
| 3 | A10 | Toggle | Advances the design example to the next higher resource utilization, `node_i_nperc_next`. |
| 4 | B10 | Press and Hold | Enables the outputs to toggle, node `i_noutput_ena`. |

Tables 4–2 and 4–3 describe how the LEDs indicate the design example's current power state.

*Table 4–2. LEDs Power State (Frequency)*

| Displays | LEDs | | State | Clock Frequency (MHz) |
|---|---|---|---|---|
| | MSB | LSB | | |
| Frequency | LED2 | LED1 | 00 | 0 |
| | | | 01 | 33 |
| | | | 10 | 67 |
| | | | 11 | 100 |

*Table 4–3. LEDs Power State (Resources)*

| Displays | LEDs | | State | % of Design Used |
|---|---|---|---|---|
| | MSB | LSB | | |
| Resources | LED4 | LED3 | 00 | 25% |
| | | | 01 | 50% |
| | | | 10 | 75% |
| | | | 11 | 100% |

The design used for power measurement is a replicated set of randomly filled ROMs that feed a multiplier block and a shift register that is fed by a signal that changes every clock cycle. The states shown in Tables 4–2 and 4–3 represent the percent of the full design used. As compiled, this full design uses:

- Logic elements: 22,493/24,624 (91%)
- Combinational functions: 1,961/24,624 (8%)
- Dedicated logic registers: 21,133/24,624 (86%)
- Total registers: 21,133
- Total pins: 73/216 (34%)
- Total memory bits: 524,288/608,256 (86%)
- Embedded Multiplier 9-bit elements: 128/132 (97 %)
- Total PLLs: 1/4 (25%)

## Measuring Power

The design example can be located by default in *<kit install>***Examples\CIII_Power_Demo**. Configure the FPGA with the SOF found in the directory.

The input clock (`i_clk` PIN_B9) is the 50-MHz oscillator on the board, which generates the input clock for the reference design through a PLL

For more information on configuring the FPGA, refer to "FPGA Configuration" on page 2–3.

Current sense resistors (0.010 Ohms +/- 1%) are installed at location JP6 (FPGA core power) and JP3 (FPGA I/O power + other device I/O power). With a digital multimeter set to the mV measurement range, the resistor at location JP6 can be used to measure the core power. The resistor at location JP3 can be used to measure the I/O power.

To obtain the power (P) in milliwatts, measure <*Measured Voltage*> (the voltage across the sense resistors at JP6 or JP3) in mV and calculate the nominal power using the equation:

P = 100 x <*Measured Voltage*> x <*Supply Voltage*>

where <*Supply Voltage*> is 1.2 V for JP6 and 2.5 V for JP3.

Advance through the various button options as outlined in Table 4–2. Notice how current increases as frequency and resource usage increase.

You can also measure the I/O power consumed by measuring the voltage across sense-resistor JP3 when Button 4 is pressed and held. Because this 2.5-V power rail is shared with other devices, there is a nominal 100 mW that must be subtracted from the calculated I/O power to obtain the FPGA I/O power.

The number of I/O pins used is controlled by the resource state (shown in Tables 4–2 and 4–3). For each increment in resources, 16 additional I/O pins are added (see Table 4–4).

*Table 4–4. I/O Pin & Resource State*

| LED4/LED3 | Number of I/O Pins |
|---|---|
| 00 | 16 |
| 01 | 32 |
| 10 | 48 |
| 11 | 64 |

Similarly, the toggle-frequency of these I/O pins is set by the overall design frequency (see Table 4–1).

## Changing the Design Example

The source code for the Cyclone III power design example is also provided so you can use it as a starting point for your own measurements. The number of outputs can be adjusted by changing parameter NUM_OUTPUTS_PER_STAMP. The default is 16, which for four resource percentage steps equates to 16 x 4 = 64.

The appropriate pins to be used as outputs are pre-assigned to the HSMC connector J1. If you would like to look at more than the 76 I/Os available on J1, you need to make the appropriate pin assignments.

# 5. Appendix: Programming the Configuration Flash Device

## Overview

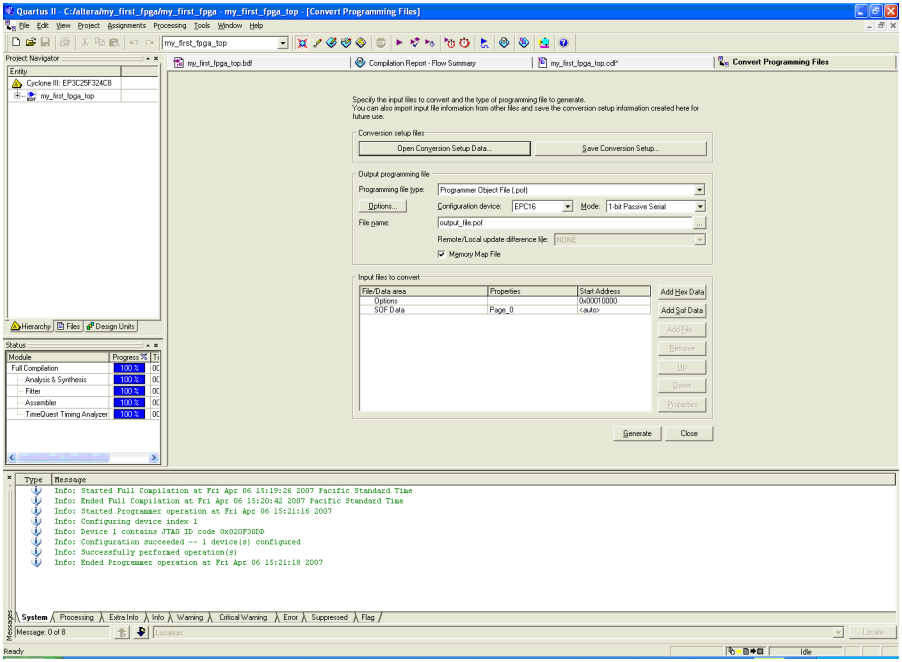
The Intel® P30 flash device uses Active Parallel Flash Configuration to configure the Cyclone® III device on power up. The Cyclone III Starter Board has a factory default configuration programmed into the P30 flash; however, once you have developed your own project, you may want to replace this factory default configuration with your own. This appendix describes how to reprogram the Intel P30 flash device.

## Creating a Flash-Programmable POF File

After Quartus II compilation, a Programmer Object File (POF) is created. Before you can program this file into the Intel P30 flash device on the Cyclone III Starter Board, you must convert it into a modified POF that the flash programmer can use to program the flash device. Perform the following steps to convert the file:

1. Choose **Convert Programming File** (File menu). The **Convert Programming Files** window opens (see Figure 5–1).

*Figure 5–1. Convert Programming Files Window*



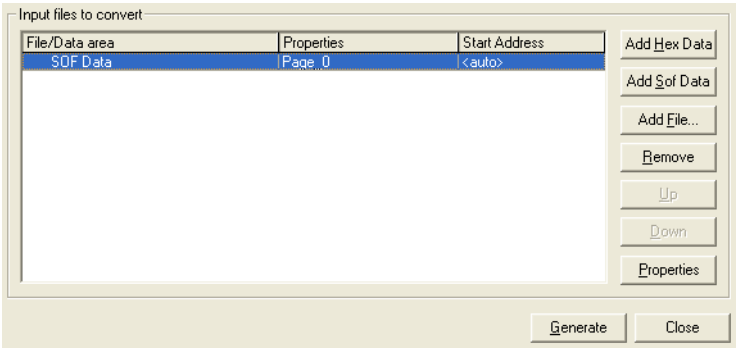

2. Make the following settings:

   - **Programming File Type:** Programmer Object File (POF)
   - **Mode:** Active Parallel Configuration
   - **Device:** CFI_128MB
   - **File Name:** Type the name of the flashable POF to write

   If you choose to overwrite the existing POF file, you will receive a warning message.

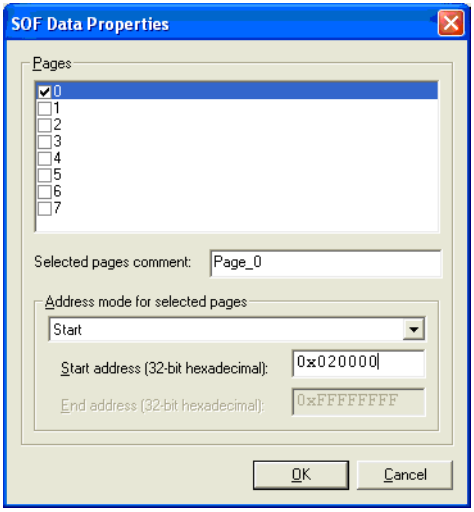
3. Under **Input file to the convert**, highlight **SOF Data**. See Figure 5–2.

*Figure 5–2. Input File to Convert*




4. Click **Add File**.
5. Choose the SOF file you want to convert and click **OK**.
6. Highlight **SOF Data** again.
7. Click **Properties**. The **SOF Data Properties** window appears.
8. Make the following settings as shown in Figure 5–3:
   - **Pages:** 0
   - **Address mode for selected pages:** Start
   - **Start address (32-bit hexadecimal):** 0x020000

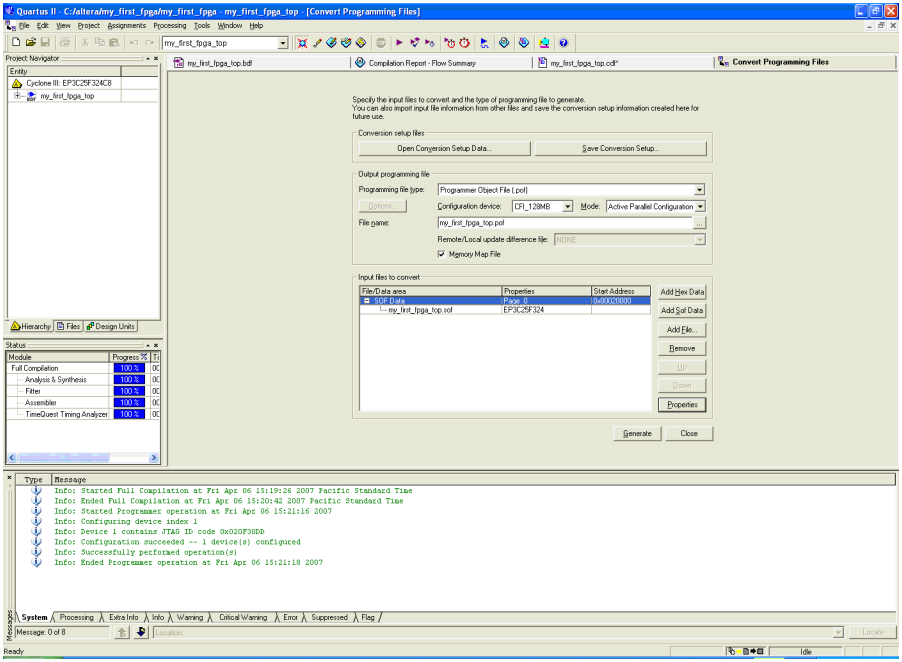
*Figure 5–3. SOF Data Properties*




Flash address 0x20000 is the default starting address from which the Cyclone III device starts loading configuration data.

9. Click **OK**. Figure 5–4 shows the updated **Convert Programming Files** window.

*Figure 5–4. Updated Convert Programming Files Window*




10. Click **Generate**. If you are overwriting the input POF you will receive a warning asking if you want to overwrite it. Click **Yes** to overwrite the file or enter a different filename. When the Quartus II software finishes converting the file, you can use the converted POF to program the on-board parallel flash device.

The Quartus II software also generates a MAP file, which can help you debug issues with locations in the flash device.

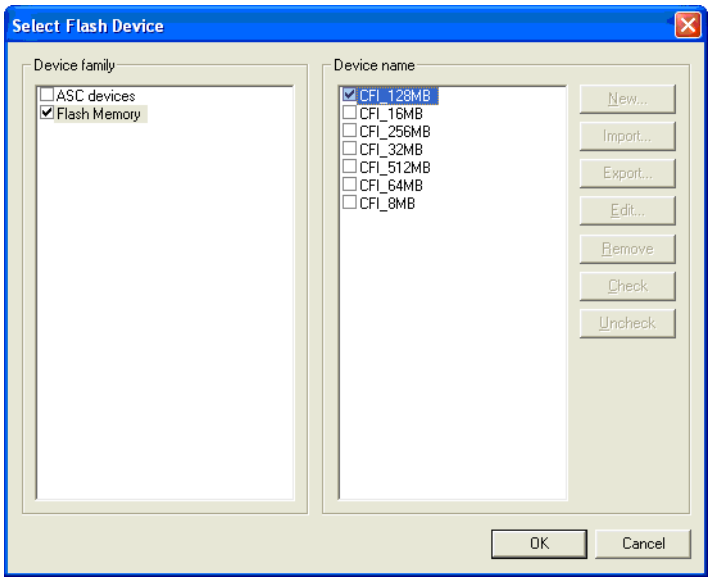
## Programming the Flash Device

To program the flash device, perform the following steps:

1. Open the Quartus II Programmer.
2. Click **Auto Detect** from the button list to the left of the programming file list area.
3. Select the detected Cyclone III 3C25 device.
4. Choose **Attach Flash Device** (Edit menu). The **Select Flash Device** window opens.

5. Turn on the **Flash Memory** and **CFI_128MB** options. (see Figure 5–5).

*Figure 5–5. Select Flash Device*




6. Click **OK**.

7. In the Programmer, highlight the CFI_128MB device.

8. Click **Change File** from the button list to the left of the programming file area.

9. Select the converted POF that you generated in the previous section.

10. Turn on the **Program/Configure** option for all devices shown in the Programmer.

Turning on the option for the POFs enables all three options, which is what you want to do. See Figure 5–6.

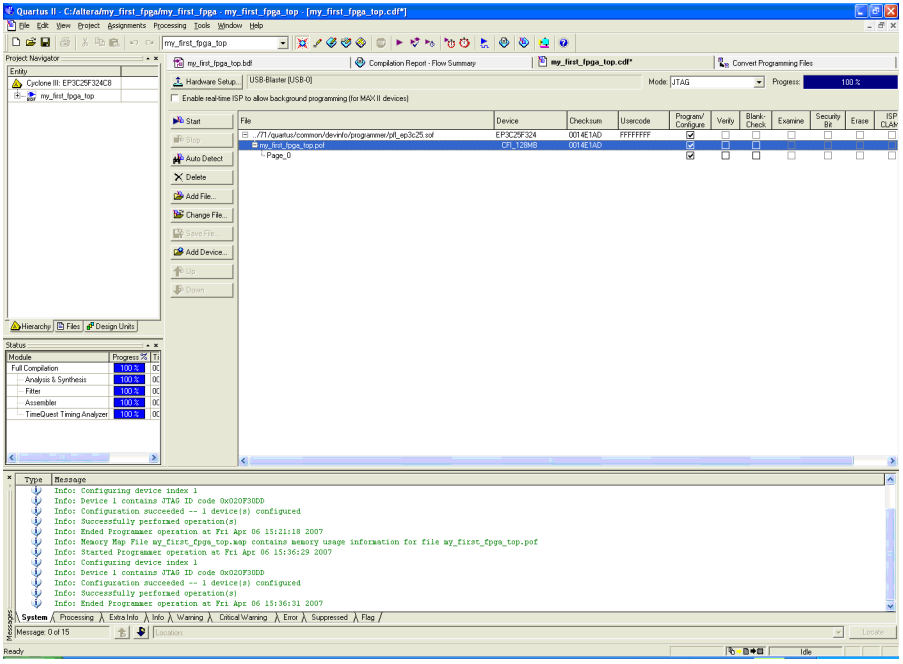
*Figure 5–6. POF Options*

| File | Device | Checksum | Usercode | Program/ Configure | Verify | Blank-Check | Examine | Security Bit | Erase | ISP CLAMP |
|---|---|---|---|---|---|---|---|---|---|---|
| Factory default PFL image | EP3C25 | 00000000 | FFFFFFFF | ☑ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| my_first_fpga_top.pof | CFI_128MB | 00000000 | | ☑ | ☐ | ☐ | | | | |
| Page_0 | | | | ☑ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |

11. Click **Start**. The Programmer loads the special flash programming hardware into the FPGA, which allows the Programmer to communicate with the flash device. The Programmer sends the POF to the flash device via the flash programming hardware. The Quartus II Message window displays the bank addresses as they are erased and then written.

    Figure 5–7 shows the Programmer when programming completes.

*Figure 5–7. Programming Complete*



12. Turn the Cyclone III Starter Board off and then on again. When the board powers up, the Cyclone III device configures with your design from the on-board flash device.

13. Push the reconfiguration button to reload the FPGA with the new flash contents.